IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In application of:

: Group Art Unit:

Seung-moon Yoo

Serial No.: Unknown

: Intellectual Property Law Department

Filed: Unknown

: International Business Machines Corp.

Title: Methods and Arrangements for

Enhancing Domino Logic

: 11400 Burnet Road

: Austin, Texas 78758

Date: August 21, 2003

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents Washington, D. C. 20231

Sir:

Applicants submit herewith patents, publications or other information of which they are aware, which they believe may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR 1.56.

While this Information Disclosure Statement may be "material" pursuant to 37 CFR 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

PATENT

In accordance with 37 CFR 1.97(g) the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56 (a) exists.

The attached form, PTO-1449, provides a listing of patents, publications, or other information as required by 37 CFR 1.98 (a)(1).

A copy of each of the items on PTO-1449 is supplied herewith.

Respectfully submitted,

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PTO/SB/08B (04-03)

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STATEMENT BY APPLICANT				First Named Inventor	SEUNG-MOON YOO		
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Sheet	1	of	1	Attorney Docket Number	AUS920030534US1		

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		ANIS, M.H. et. al, "Energy-Efficient noise-Tolerant Dynamic Styles for Scaled-Down CMOS and MTCMOS Technologies", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, April 2002, pp. 71-78, v. 10, n. 2, IEEE, United States (Publisher Item Id. S 1063-8210(02)00485-7).	

Examiner	Date	[
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